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1 Computing curricula 2001

September 2001 **Journal on Educational Resources in Computing (JERIC)**

Full text available: pdf(613.63 KB) html(2.78 KB) Additional Information: full citation, references, citings, index terms

2 Testing and Debugging Custom Integrated Circuits

Edward H. Frank, Robert F. Sproull

December 1981 **ACM Computing Surveys (CSUR)**, Volume 13 Issue 4

Full text available: pdf(2.25 MB) Additional Information: full citation, references, citings, index terms

3 From Electron Mobility to Logical Structure: A View of Integrated Circuits

Wesley A. Clark

September 1980 **ACM Computing Surveys (CSUR)**, Volume 12 Issue 3

Full text available: pdf(3.29 MB) Additional Information: full citation, references, citings, index terms

4 Evaluation of a Commercial Microprocessor

Robert Yung

June 1998 Technical Report, Sun Microsystems, Inc.

Full text available: pdf(595.89 KB) Additional Information: full citation, abstract

A dissertation submitted in partial satisfaction of the requirements for the degree of Doctor of Philosophy in Computer Science in the Graduate Division of the University of California, Berkeley.

5 MIXS: A mixed level simulator for large digital system logic verification

Tohru Sasaki, Akihiko Yamada, Shunichi Kato, Terufumi Nakazawa, Kyoji Tomita, Nobuyoshi Nomizu

June 1980 **Proceedings of the seventeenth design automation conference on Design automation**

Full text available: pdf(567.02 KB) Additional Information: full citation, abstract, references, citings, index terms

A mixed level simulator, MIXS, is a logic verification tool which has multiple simulation capabilities. Main MIXS techniques are time wheel and selective trace algorithm for functional level simulation based on 'node' model concept and the linkage function of functional models, described in different detail, with network information. The mixed level simulation for large digital systems can be achieved very efficiently by using the above techniques.

6 A personal view of the personal work station: some firsts in the Fifties

Douglas Ross

January 1986 **Proceedings of the ACM Conference on The history of personal workstations**

Full text available: pdf(4.26 MB) Additional Information: full citation, references, index terms

7 Logic simulation for LSI

Kazuyuki Hirakawa, Noboru Shiraki, Michiaki Muraoka

January 1982 **Proceedings of the nineteenth design automation conference**

Full text available: pdf(470.96 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper describes the logic simulation system and the design verification method for logic design, timing analysis, and testing for VLSI. The integrity of test and network data on a logic design stage must be kept in LSI testing in the final verification stage. In dealing with consistency, emphasis is placed on the discrepancy between the real time domain on a simulator and a testing time domain on an LSI tester. The logic simulation system (Block INtegrator and AnaLYzer: BINALY) handles ...

8 A new string search hardware architecture for VLSI

K. Takahashi, H. Yamada, H. Nagai, K. Matsumi

June 1986 **ACM SIGARCH Computer Architecture News , Proceedings of the 13th annual international symposium on Computer architecture**, Volume 14 Issue 2

Full text available: pdf(683.39 KB) Additional Information: full citation, abstract, references, index terms

This paper presents a new architecture for practical string search hardware design. This architecture is based on the finite state automaton design concept using a character control charge transfer model. The resultant hardware is a set of programmable sequential logic (PSL) circuits, each of which consists of a sequential logic and memory parts. The logic part is an array of logical gates, each of which is controlled by the read-out signal from the memory part, to connect the flip-flops. T ...

9 Formal verification of pipeline control using controlled token nets and abstract interpretation

Pei-Hsin Ho, Adrian J. Isles, Timothy Kam

November 1998 **Proceedings of the 1998 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(1.02 MB) Additional Information: full citation, references, citings, index terms

Keywords: abstract interpretation, computer-aided design, controlled token net, formal verification, functional verification, model checking, pipeline control verification, processor verification

10 Programmable applications: interpreter meets interface

Michael Eisenberg
April 1995 **ACM SIGCHI Bulletin**, Volume 27 Issue 2

Full text available: pdf(4.42 MB) Additional Information: full citation, abstract, citings, index terms

Current fashion in "user-friendly" software design tends to place an over-reliance on direct manipulation interfaces. To be truly expressive (and thus truly user-friendly), applications need both learnable interfaces and domain-enriched languages that are accessible to the user. This paper discusses some of the design issues that arise in the creation of such *programmable applications.* As an example, we present "SchemePaint," a graphics application that combines a MacPaint-like interface ...

11 Computing as a discipline

D. E. Comer, David Gries, Michael C. Mulder, Allen Tucker, A. Joe Turner, Paul R. Young
February 1989 **Communications of the ACM**, Volume 32 Issue 1

Full text available: pdf(1.68 MB) Additional Information: full citation, abstract, references, citings, index terms

The final report of the Task Force on the Core of Computer Science presents a new intellectual framework for the discipline of computing and a new basis for computing curricula. This report has been endorsed and approved for release by the ACM Education Board.

12 An expert system application in semicustom VLSI design

R. L. Steele
October 1987 **24th ACM/IEEE conference proceedings on Design automation conference**

Full text available: pdf(815.63 KB) Additional Information: full citation, abstract, references, index terms

This paper describes the implementation of a prototype expert system that provides standard cell design advice in the areas of performance, manufacturability, testability, and overall design quality, from a netlist description of an application specific integrated circuit (ASIC) design. The system is currently being developed on a Symbolics Lisp Machine using a hybrid AI programming language, called Proteus. The language integrates both known and novel AI programming techniques i ...

13 Electronic Computers: A Historical Survey

Saul Rosen
January 1969 **ACM Computing Surveys (CSUR)**, Volume 1 Issue 1

Full text available: pdf(2.45 MB) Additional Information: full citation, references, citings, index terms

14 A fast routability-driven router for FPGAs

Jordan S. Swartz, Vaughn Betz, Jonathan Rose
March 1998 **Proceedings of the 1998 ACM/SIGDA sixth international symposium on Field programmable gate arrays**

Full text available: pdf(1.12 MB) Additional Information: full citation, abstract, references, citings, index terms

Three factors are driving the demand for rapid FPGA compilation. First, as FPGAs have grown in logic capacity, the compile computation has grown more quickly than the compute power of the available computers. Second, there exists a subset of users who are willing to pay for very high speed compile with a decrease in quality of result, and accordingly being required to use a larger FPGA or use more real-estate on a given FPGA than is otherwise necessary. Third, very high speed compile has be ...

15

A computer science syllabus for gifted pre-college students
Richard E. Korf
February 1983 **ACM SIGCSE Bulletin , Proceedings of the fourteenth SIGCSE technical symposium on Computer science education**, Volume 15 Issue 1
Full text available: pdf(347.91 KB) Additional Information: full citation, abstract, references, index terms

A computer science syllabus was designed for and taught to a group of gifted and talented high school students. A core course included segments on programming in LISP, software systems, digital hardware, theoretical computer science, and artificial intelligence. In addition, some students elected an independent programming project course. It was found that gifted pre-college students can be taught computer science, as opposed to merely computer programming.

16 Physical Design: Integrated retiming and placement for field programmable gate arrays
Deshanand P. Singh, Stephen D. Brown
February 2002 **Proceedings of the 2002 ACM/SIGDA tenth international symposium on Field-programmable gate arrays**
Full text available: pdf(285.51 KB) Additional Information: full citation, abstract, references, citings

Retiming is a synchronous circuit transformation that can optimize the delay of a synchronous circuit by moving registers across combinational circuit elements. The combinational structure remains unchanged and the observable behavior of the circuit is identical to the original.In this paper, we address the problem of applying retiming techniques to circuits implemented in Field Programmable Gate Arrays (FPGAs). FPGAs contain prefabricated and configurable routing elements that allow us to easil ...

17 ITiCSE 2000 working group reports: Distributed expertise for teaching computer organization & architecture
Lillian (Boots) Cassel, Mark Holliday, Deepak Kumar, John Impagliazzo, Kevin Bolding, Murray Pearson, Jim Davies, Gregory S. Wolffe, William Yurcik
June 2001 **ACM SIGCSE Bulletin**, Volume 33 Issue 2
Full text available: pdf(1.89 MB) Additional Information: full citation, abstract, references, citings

This report presents preliminary results from our project on creating distributed expertise for teaching computer organization & architecture course(s) in the undergraduate computer science curriculum. We present the details of an online survey designed to gather information from faculty on the current state of teaching this course. The survey also tries to identify specific areas of need for creating distributed expertise as reported by various faculty. We also present several resources that ha ...

18 ITiCSE 2000 working group reports: Distributed expertise for teaching computer organization & architecture
Lillian (Boots) Cassel, Mark Holliday, Deepak Kumar, John Impagliazzo, Kevin Bolding, Murray Pearson, Jim Davies, Gregory S. Wolffe, William Yurcik
June 2001 **Working group reports from ITiCSE on Innovation and technology in computer science education**
Full text available: pdf(1.89 MB) Additional Information: full citation, abstract, references, citings, index terms

This report presents preliminary results from our project on creating distributed expertise for teaching computer organization & architecture course(s) in the undergraduate computer science curriculum. We present the details of an online survey designed to gather information from faculty on the current state of teaching this course. The survey also tries to identify specific areas of need for creating distributed expertise as reported by various faculty. We also present several resources that ha ...

19

High Rate Soft Output Viterbi Decoder

Eric Luthi, Emmanuel Casseau

March 1996 **Proceedings of the 1996 European conference on Design and Test**

Full text available: pdf(621.37 KB) Publisher Site Additional Information: full citation, abstract

This paper presents the architecture of a high rate soft output Viterbi decoder (100 Mb/s for worst case process conditions, 8 states, coding rate R=1/2, using a 0.6ym CMOS technology), using the "radix" trellis method (collapsed trellis) to speed up the rate of a soft output decoder using the Viterbi algorithm and the a posteriori weighting algorithm. The size of this circuit is roughly twice that of the original soft output Viterbi decoder while the speed is increased by a factor of 2. Because ...

Keywords: digital communication systems, high data rates, Viterbi decoding, soft output Viterbi decoding, collapsed trellis, VLSI design

20 Status of computer sciences curricula in colleges and universities

William F. Atchison, John W. Hamblen

April 1964 **Communications of the ACM**, Volume 7 Issue 4

Full text available: pdf(303.20 KB) Additional Information: full citation, citings, index terms

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12	BRS	L12	43	(circuit adj design.ti.) and errors and (finding or locating or correcting)	USPAT	2004/05/19 14:08
13	BRS	L13	2	(circuit adj design.ti.) and errors.ti.	USPAT	2004/05/19 14:09
14	BRS	L14	2	locating and (digital adj circuits) near errors	USPAT	2004/05/19 14:10
15	BRS	L15	0	locating and (digital adj circuits) near errors and (D adj flip adj flops)	USPAT	2004/05/19 14:11
16	BRS	L16	13	locating and (digital adj circuits) and errors and (D adj flip adj flops)	USPAT	2004/05/19 14:11
17	BRS	L17	8	(locating and errors).ti.	USPAT	2004/05/19 14:13
18	BRS	L18	0	(locating and errors).ti. and (digital adj circuit)	USPAT	2004/05/19 14:13
19	BRS	L19	0	(locating adj errors).ti. and (digital adj circuit)	USPAT	2004/05/19 14:13
20	BRS	L20	3	(locating adj errors) and (digital adj circuit)	USPAT	2004/05/19 15:09
21	BRS	L21	0	(digital adj circuit) and mistakes and (lithographic adj masks) and	USPAT	2004/05/19 15:10
22	BRS	L22	0	(digital adj circuit) and mistakes and (lithographic adj masks)	USPAT	2004/05/19 15:10

	Type	L #	Hits	Search Text	DBs	Time Stamp
23	BRS	L23	10	(digital adj circuit) and (lithographic adj masks)	USPAT	2004/05/19 15:10